UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,872	02/27/2002	Eric DeLano	10016663-1	4721

7590 11/05/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,872	DELANO, ERIC	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been considered.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "104(1)" has been used to designate the Program Counters for Clusters 102(1), 102(2), and 102(N). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because there is a header found on each page of the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: Please correct page 5, paragraph 1, last line from "to the register file *204* of the other core..." to read --to the register file 304 of the other core...--. Appropriate correction is required.

Claim Objections

5. Claim 17 is objected to because of the following informalities: Please correct claim 9, lines 6-7 from "...one of the clusters in the *wide* mode of operation." To read --...one of the clusters in the throughput mode of operation." Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what the claim is bypassing.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being taught by Batten et al., U.S. Patent Number 6,269,439 (herein referred to as Batten).

10. Referring to claim 1, Batten has taught a method for processing bundled instructions through execution units of a processor, comprising the steps of:

a. Fetching a first bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the first bundle to a first cluster of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

c. Fetching a second bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

d. Distributing the second bundle to a second cluster of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

11. Referring to claim 2, Batten has taught processing the first bundle within the first cluster (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

12. Referring to claim 3, Batten has taught processing the second bundle within the second cluster (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

13. Referring to claim 4, Batten has taught architecting data from the first cluster to a first register file (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15 and 24-29; and Figures 12 and 13).

14. Referring to claim 5, Batten has taught committing architected state from the second cluster to the first register file (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15 and 24-29; and Figures 12 and 13).

15. Referring to claim 6, Batten has taught architecting data from the second cluster to a second register file (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15 and 24-29; and Figures 12 and 13).

16. Referring to claim 7, Batten has taught fetching the first bundle comprising decoding instructions into the first bundle of the singly-threaded instructions (Batten column 11, lines 1-15 and Figure 12).

17. Referring to claim 8, Batten has taught fetching the second bundle comprising decoding instructions into the second bundle of the singly-threaded instructions (Batten column 11, lines 1-15 and Figure 12).

18. Referring to claim 9, Batten has taught

a. Fetching a third bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the third bundle to the first and second clusters of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

c. Bypassing data between the clusters, as needed, to facilitate processing of the third bundle through the clusters (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 6, line 6).

19. Referring to claim 10, Batten has taught utilizing a latch to couple the data between the clusters (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 6, line 6). In regards to Batten, the file replication technique and cooperative interconnection technique requires the data to be moved from private cluster registers to global registers before the destination cluster can read the data and move/write the data into its private registers. The

intermediate, global register is a type of latch. Please see FOLDOC's definitions of "latch" and "register."

20. Referring to claim 11, Batten has taught selecting a configuration bit prior to the steps of fetching the third bundle, distributing the third bundle, and bypassing (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

21. Referring to claim 12, Batten has taught a method for processing bundled instructions through execution units of a processor, comprising the steps of:

a. Fetching a first bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the first bundle to two or more clusters of the execution units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

c. Bypassing data between the clusters, as needed, to facilitate processing of the first bundle through the clusters (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 6, line 6).

22. Referring to claim 13. Batten has taught

a. Fetching a second bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

b. Distributing the second bundle to one of the clusters for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12);

c. Fetching a third bundle of singly-threaded instructions (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12); and

d. Distributing the third bundle to another one of the clusters units for execution therethrough (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

23. Referring to claim 13, Batten has taught selecting a configuration bit prior to the steps of fetching the second bundle, distributing the second bundle, fetching a third bundle and distributing the third bundle (Batten Abstract; column 1, lines 28-32, 39-55; column 4, line 65 to column 5, line 8; column 11, lines 1-15; and Figure 12).

24. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being taught by Murata et al., U.S. Patent Number 5,729,761 (herein referred to as Murata)

25. Referring to claim 15, Murata has taught in a processor architecture of the type having two or more clusters of execution units for processing instructions (Murata column 1, line 54 to column 2, line 19; column 2, line 56 to column 3, line 17; and Figure 1), the improvement comprising a thread decoder for grouping instructions into singly threaded bundles and for distributing the bundles to the clusters according to either a wide mode or throughput mode of operation (Murata column 1, line 54 to column 2, line 19; column 3, lines 44-55; column 4, lines

60 to column 4, line 6; column 4, lines 15-26 and 33-52; column 9, lines 6-26 and 49-62; Figure 3; Figure 4; Figure 5; Figure 10; Figure 11; and Figure 12).

26. Referring to claim 16, Murata has taught wherein each cluster comprises a core and register file (Murata column 1, line 54 to column 2, line 19; column 2, line 56 to column 3, line 17; and Figure 1).

27. Referring to claim 17, Murata has taught wherein the thread decoder distributes bundles of singly-threaded instructions through a multiple of clusters in the wide mode of operation, and wherein the thread decoder distributes bundles of singly-threaded instructions through one of the clusters in the throughput mode of operation (Murata column 1, line 54 to column 2, line 19; column 3, lines 44-55; column 4, lines 60 to column 4, line 6; column 4, lines 15-26 and 33-52; column 9, lines 6-26 and 49-62; Figure 3; Figure 4; Figure 5; Figure 10; Figure 11; and Figure 12).

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Panwar et al., U.S. Patent Number 6,098,165, has taught a multiple cluster system with local memory, shared memory, and a bypass mechanism.

b. Arora et al., U.S. Patent Number 6,629,232, has taught a multiple cluster system with shared memory.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
1 November 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100